Data Sheet

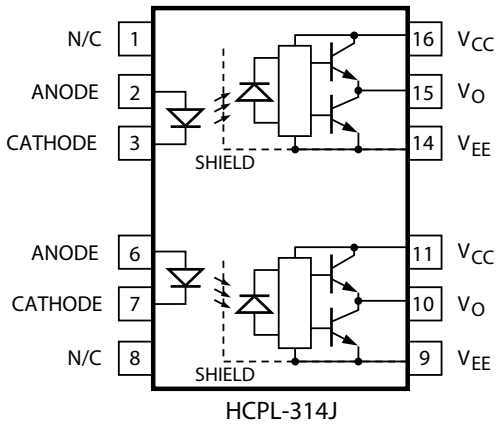
HCPL-314J

0.4-Amp Output Current IGBT Gate Drive Optocoupler

Description

The HCPL-314J family of devices consists of an AlGaAs LED optically coupled to an integrated circuit with a power output stage. These optocouplers are ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by this optocoupler makes it ideally suited for directly driving small or medium power IGBTs. For IGBTs with higher ratings, the HCPL-3150(0.5A) or HCPL-3120 (2.0A) optocouplers can be used.

Figure 1: Functional Diagram



HCPL-314J

Table 1: Truth Table

LED	VO
OFF	LOW
ON	HIGH

A 0.1-µF bypass capacitor must be connected between pins V_{CC} and V_{EE}.

Features

- 0.4-A minimum peak output current
- High-speed response:
  0.7-µs max. propagation delay over temp. range
- Ultra-high CMR: min. 25 kV/µs at V_{CM} = 1.5 kV
- Bootstrappable supply current: max. 3 mA
- Wide operating temp. range: –40°C to 100°C
- Wide V_{CC} operating range: 10V to 30V over temp. range
- Available in DIP8 (single) and SO16 (dual) package
- Safety approvals:
  UL recognized, 5000 V_{rms} for 1 minute. CSA approval.
  IEC/EN/DIN EN 60747-5-5 approval V_{IORM} = 1414 V_{peak}

Applications

- Isolated IGBT/power MOSFET gate drive
- AC and brushless DC motor drives
- Inverters for appliances
- Industrial inverters
- Switch Mode Power Supplies (SMPS)
- Uninterruptable Power Supplies (UPS)

Selection Guide

Package Type	Part Number	Number of Channels
SO16	HCPL-314J	2

CAUTION! It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Ordering Information

HCPL-314J is UL recognized with 5000 V_{rms} for 1 minute per UL1577.

Part Number	Option		Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant	Non RoHS Compliant					
HCPL-314J	-000E	No option	SO-16	X		X	45 per tube
	-500E	#500		X	X	X	850 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-314J-500E to order product of SO-16 Surface Mount package in Tape and Reel packaging with IEC/EN/ DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Example 2:

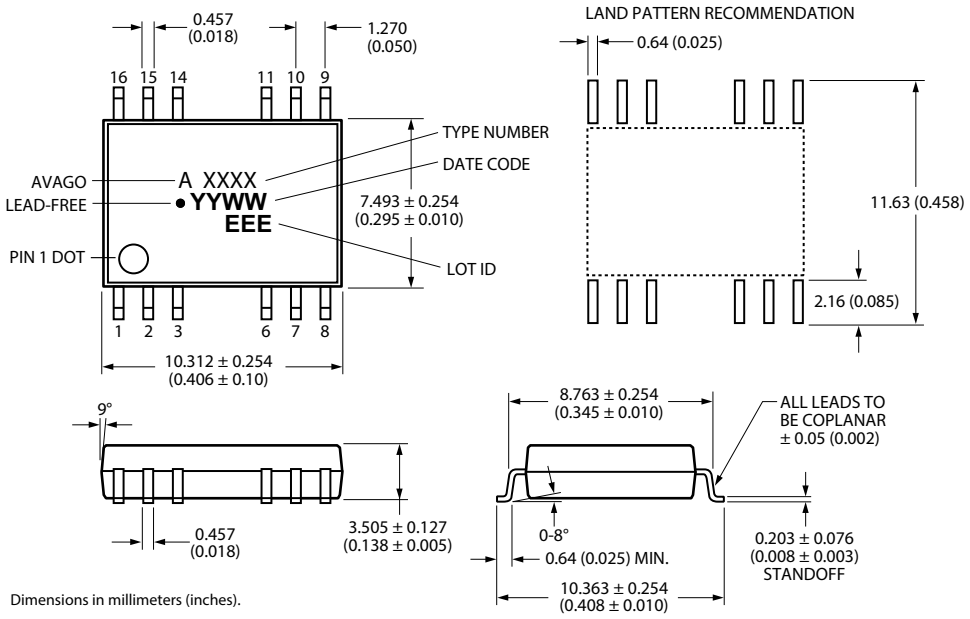
HCPL-314J to order product of SO-16 Surface Mount package in tube packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval and non RoHS compliant.

Option data sheets are available. Contact your Broadcom® sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, whereas (new) products launched since July 15, 2001 and RoHS compliant option will use '-XXXE'.

Package Outline Drawing

Figure 2: 16-Lead Surface Mount Package



Dimensions in millimeters (inches).

Floating lead protrusion is 0.25 mm (10 mils) max.

Note: Initial and continued variation in color of the white mold compound is normal and does not affect performance or reliability of the device.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The HCPL-314J has been approved by the following organizations:

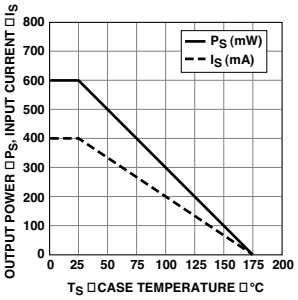
IEC/EN/DIN EN 60747-5-5	Approval under: DIN EN 60747-5-5 (VDE 0884-5):2011-11 EN 60747-5-5:2011.
UL	Approval under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS}. File E55361.
CSA	Approval under CSA Component Acceptance Notice #5, File CA 88324.

Table 2: IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1	—		—
for rated mains voltage ≤ 150 V_{rms}		I - IV	
for rated mains voltage ≤ 300 V_{rms}		I - IV	
for rated mains voltage ≤ 600 V_{rms}		I - IV	
for rated mains voltage ≤ 1000 V_{rms}		I - III	
Climatic Classification	—	55/100/21	—
Pollution Degree (DIN VDE 0110/1.89)	—	2	—
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{peak}
Input to Output Test Voltage, Method b[a] V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2652	V_{peak}
Input to Output Test Voltage, Method a[a] V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	2262	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	V_{peak}
Safety-limiting values - maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current[b]	$I_{S, INPUT}$	400	mA
Output Power[b]	$P_{S, OUTPUT}$	1200	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$>10^9$	Ω

a. Refer to the IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the Avago Regulatory Guide to Isolation Circuits, AV02-2041EN, for a detailed description of Method a and Method b partial discharge test profiles.

b. See the following figure for dependence of P_S and I_S on ambient temperature.



Insulation and Safety Related Specifications

Parameter	Symbol	HCPL-314J	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group	—	IIIa	—	Material Group (DIN VDE 0110, 1/89, Table 1)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	–55	125	°C	
Operating Temperature	T_A	–40	100	°C	
Average Input Current	$I_{F(AVG)}$	—	25	mA	a
Peak Transient Input Current (<1 µs pulse width, 300 pps)	$I_{F(TRAN)}$	—	1.0	A	
Reverse Input Voltage	V_R	—	5	V	
"High" Peak Output Current	$I_{OH(PEAK)}$	—	0.6	A	b
"Low" Peak Output Current	$I_{OL(PEAK)}$	—	0.6	A	b
Supply Voltage	V_{CC}-V_{EE}	–0.5	35	V	
Output Voltage	$V_{O(PEAK)}$	–0.5	V_{CC}	V	
Output Power Dissipation	P_O	—	260	mW	c
Input Power Dissipation	P_I	—	105	mW	d
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane.				
Solder Reflow Temperature Profile	See the Package Outline Drawing section.				

a. Derate linearly above 70°C free air temperature at a rate of 0.3 mA/°C.

b. Maximum pulse width = 10 µs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 0.4A. See the Applications Information section for additional details on limiting I_{OL} peak.

c. Derate linearly above 85°C, free air temperature at the rate of 4.0 mW/°C.

d. Input power dissipation does not require derating.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Power Supply	V_{CC}-V_{EE}	10	30	V	
Input Current (ON)	$I_{F(ON)}$	8	12	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	–3.6	0.8	V	
Operating Temperature	T_A	–40	100	°C	

Electrical Specifications (DC)

Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}	0.2	—	—	A	$V_O = V_{CC} - 4$	4	a
		—	0.4	0.5	—	$V_O = V_{CC} - 10$	5	b
Low Level Output Current	I_{OL}	0.2	0.4	—	A	$V_O = V_{EE} + 2.5$	7	a
		—	0.4	0.5	—	$V_O = V_{EE} + 10$	8	b
High Level Output Voltage	V_{OH}	$V_{CC} - 4$	$V_{CC} - 1.8$	—	V	$I_O = -100$ mA	3	c, d
Low Level Output Voltage	V_{OL}	—	0.4	1	V	$I_O = 100$ mA	6	
High Level Supply Current	I_{CCH}	—	0.7	3	mA	$I_O = 0$ mA	9, 10	e
Low Level Supply Current	I_{CCL}	—	1.2	3	mA	$I_O = 0$ mA		
Threshold Input Current Low to High	I_{FLH}	—	—	5	mA	$I_O = 0$ mA, $V_O > 5$V	11, 17	
Threshold Input Voltage High to Low	V_{FHL}	0.8	—	—	V	—		
Input Forward Voltage	V_F	1.2	1.5	1.8	V	$I_F = 10$ mA	18	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$	—	–1.2	—	mV/°C	—		
Input Reverse Breakdown Voltage	BV_R	3	10	—	V	$I_R = 100$ µA		
Input Capacitance	C_{IN}	—	70	—	pF	f = 1 MHz, $V_F = 0$V		

a. Maximum pulse width = 50 µs, maximum duty cycle = 0.5%.

b. Maximum pulse width = 10 µs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 0.4A. See the Applications Information section for additional details on limiting I_{OL} peak.

c. In this test, V_{OH} is measured with a DC load current. When driving capacitive load V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.

d. Maximum pulse width = 1 ms, maximum duty cycle = 20%.

e. For each channel. The power supply current increases when operating frequency and Qg of the driven IGBT increases.

Switching Specifications (AC)

Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}	0.1	0.2	0.7	µs	Rg = 47Ω, Cg = 3 nF, f = 10 kHz, Duty Cycle = 50%, I_F = 8 mA, V_{CC} = 30V	12, 13, 14, 15,	a
Propagation Delay Time to Low Output Level	t_{PHL}	0.1	0.3	0.7	µs		16, 19	
Propagation Delay Difference Between Any Two Parts or Channels	PDD	–0.5	—	0.5	µs			b
Rise Time	t_R	—	50	—	ns			
Fall Time	t_F	—	50	—	ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	25	35	—	kV/µs	T_A = 25°C, V_{CM} = 1.5 kV	20	c, d
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	25	35	—	kV/µs		20	c, e

a. This load condition approximates the gate load of a 1200V/25A IGBT.

b. PDD is the difference between t_{PHL} and t_{PLH} between any two parts or channels under the same test conditions.

c. Pins 3 and 4 (HCPL-314J) need to be connected to LED common.

d. Common mode transient immunity in the high state is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse V_{CM} to assure that the output will remain in the high state (i.e. V_O > 6.0V).

e. Common mode transient immunity in a low state is the maximum tolerable $|dV_{CM}/dt|$ of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e. V_O < 1.0V).

Package Characteristics

For each channel unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000	—	—	V_{rms}	T_A = 25°C, RH < 50% for 1 min.		a, b
Output-Output Momentary Withstand Voltage	V_{O-O}	1500	—	—	V_{rms}			c
Input-Output Resistance	R_{I-O}	—	10^{12}	—	Ω	V_{I-O} = 500V		b
Input-Output Capacitance	C_{I-O}	—	1.2	—	pF	Freq = 1 MHz		

a. In accordance with UL 1577, each HCPL-314J optocoupler is proof tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 second. This test is performed before 100% production test for partial discharge (method B) shown in Table 2, IEC/EN/DIN EN 60747-5-5 Insulation Characteristics, if applicable.

b. Device considered a two-terminal device: Pins on input side shorted together, and pins on output side shorted together.

c. Device considered a two-terminal device: Channel one output side pins shorted together, and channel two output side pins shorted together.

Figure 3: V_{OH} vs. Temperature

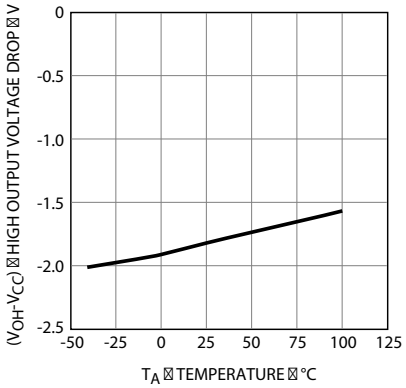


Figure 4: I_{OH} vs. Temperature

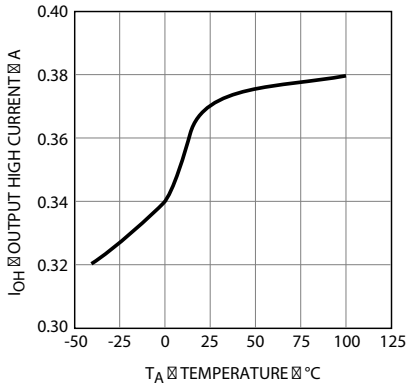


Figure 5: V_{OH} vs. I_{OH}

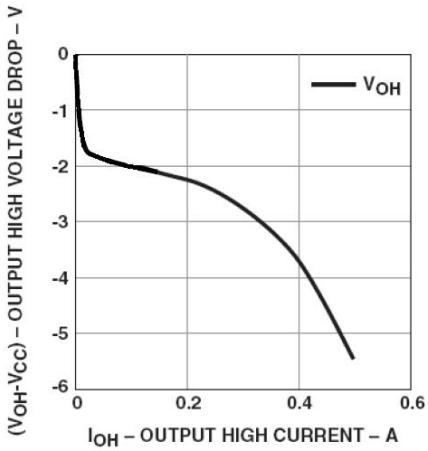


Figure 6: V_{OL} vs. Temperature

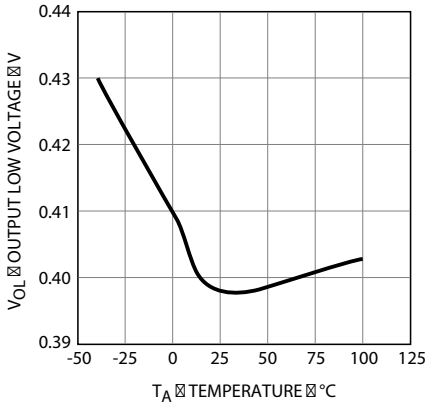


Figure 7: I_{OL} vs. Temperature

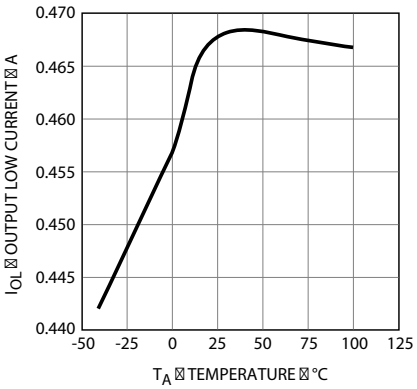


Figure 8: V_{OL} vs. I_{OL}

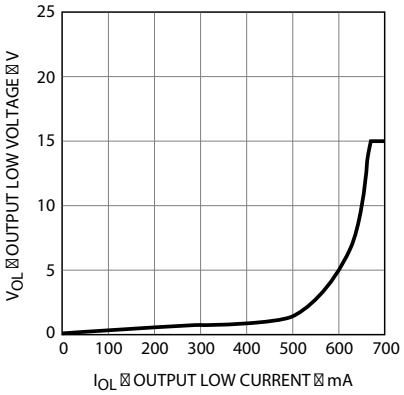


Figure 9: I_{CC} vs. Temperature

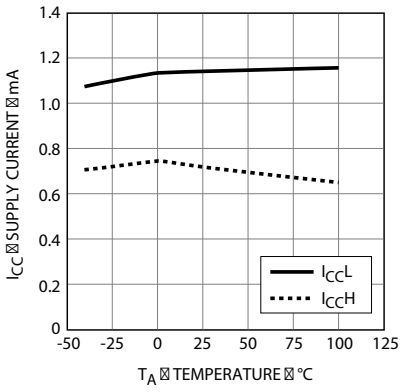


Figure 10: I_{CC} vs. V_{CC}

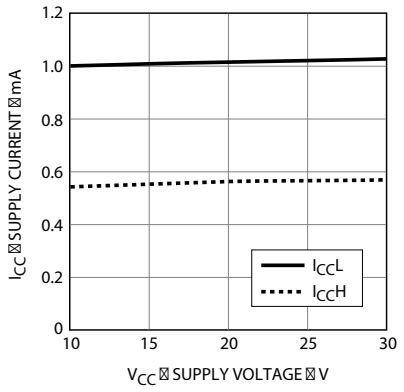


Figure 11: I_{FLH} vs. Temperature

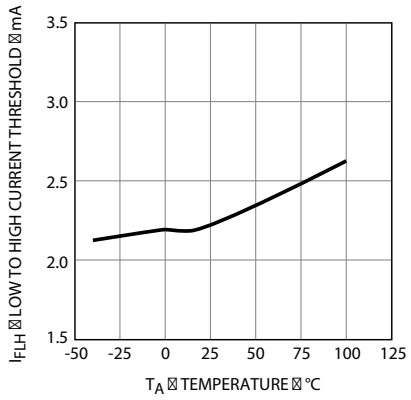


Figure 12: Propagation Delay vs. V_{CC}

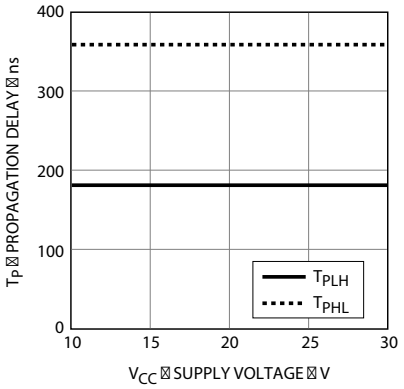


Figure 13: Propagation Delay vs. I_F

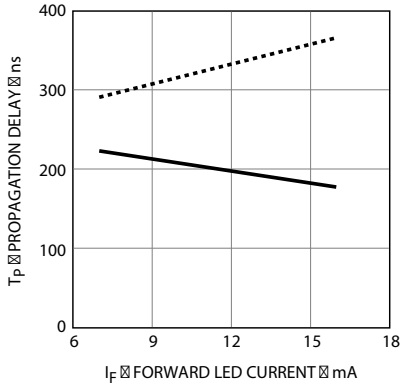


Figure 14: Propagation Delay vs. Temperature

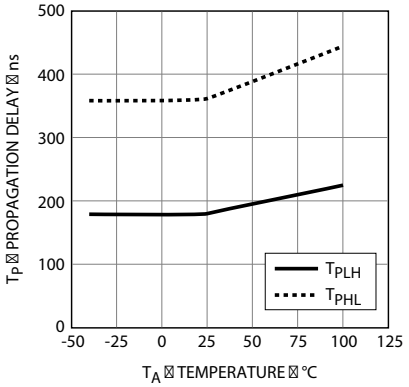


Figure 15: Propagation Delay vs. Rg

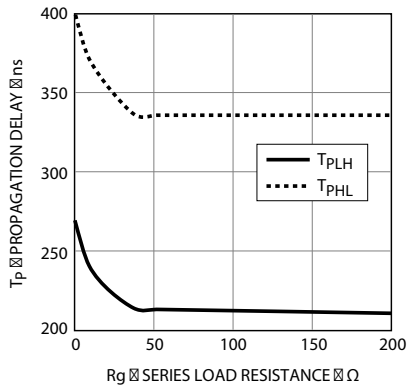


Figure 16: Propagation Delay vs. Cg

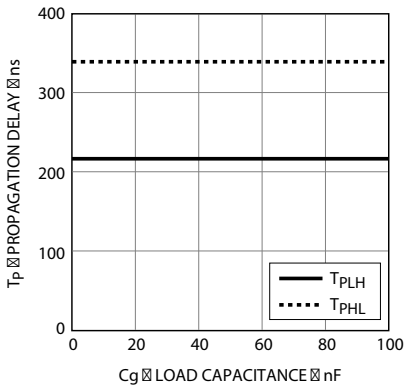


Figure 17: Transfer Characteristics

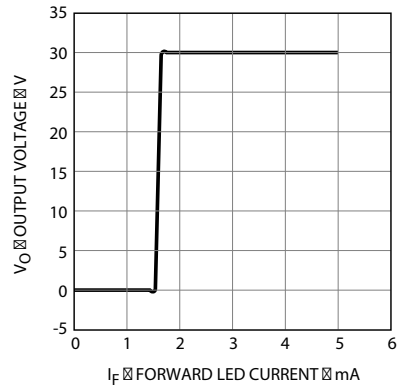


Figure 18: Input Current vs. Forward Voltage

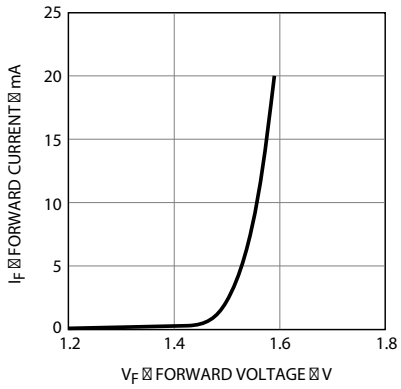


Figure 19: Propagation Delay Test Circuit and Waveforms

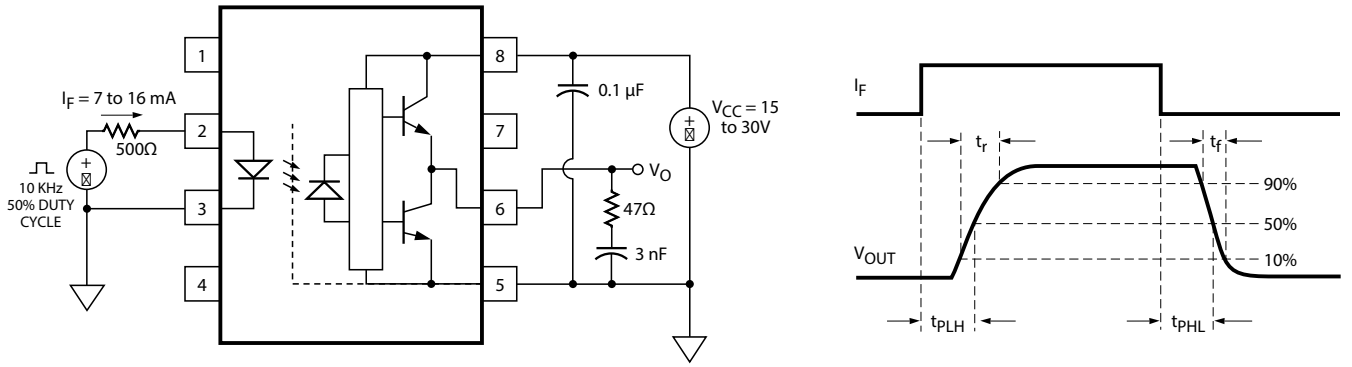
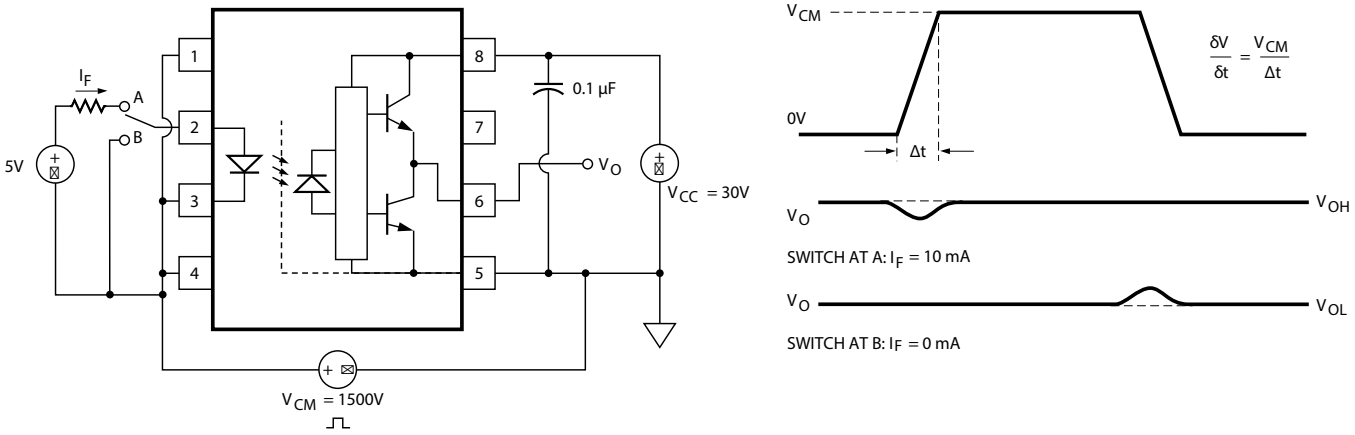


Figure 20: CMR Test Circuit and Waveforms

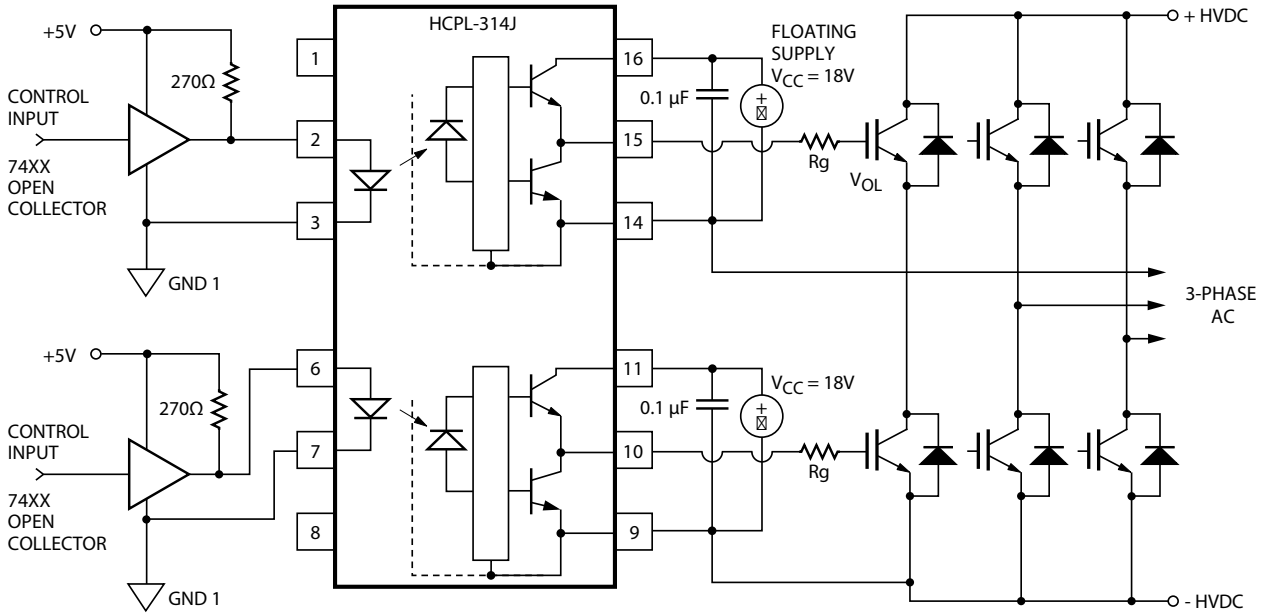


Applications Information

Eliminating Negative IGBT Gate Drive

To keep the IGBT firmly off, the HCPL-314J has a very low maximum V_{OL} specification of 1.0V. Minimizing Rg and the lead inductance from the HCPL-314J to the IGBT gate and emitter (possibly by mounting the HCPL-314J on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 21. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the HCPL-314J input as this can result in unwanted coupling of transient signals into the input of HCPL-314J and degrade performance. (If the IGBT drain must be routed near the HCPL-314J input, then the LED should be reverse biased when in the off state, to prevent the transient signals coupled from the IGBT drain from turning on the HCPL-314J.) An external clamp diode may be connected between pins 14 & 15 and pins 9 & 10 (as shown in Figure 21) for the protection of HCPL-314J in the case of IGBTs switching inductive load.

Figure 21: Recommended LED Drive and Application Circuit for HCPL-314J



Selecting the Gate Resistor (Rg)

Step 1: Calculate Rg minimum from the I_{OL} peak specification. The IGBT and Rg in Figure 26 can be analyzed as a simple RC circuit with a voltage supplied by the HCPL-314J.

$$Rg \geq \frac{V_{CC} - V_{OL}}{I_{OLPEAK}}$$

$$= \frac{24V - 5V}{0.6A}$$

$$= 32\Omega$$

The V_{OL} value of 5V in the previous equation is the V_{OL} at the peak current of 0.6A. (See Figure 8.)

Step 2: Check the HCPL-314J power dissipation and increase Rg if necessary. The HCPL-314J total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O).

$P_T = P_E + P_O$

$P_E = I_F \bullet V_F \bullet$ Duty Cycle

$P_O = P_{O(BIAS)} + P_{O(SWITCHING)} = I_{CC} \bullet V_{CC} + E_{SW}(Rg,Qg) \bullet f = (I_{CCBIAS} + K_{ICC} \bullet Qg \bullet f) \bullet V_{CC} + E_{SW}(Rg,Qg) \bullet f$

where $K_{ICC} \bullet Qg \bullet f$ is the increase in I_{CC} due to switching and K_{ICC} is a constant of 0.001 mA/(nC*kHz). For the circuit in Figure 21 with I_F (worst case) = 10 mA, Rg = 32Ω, Max Duty Cycle = 80%, Qg = 100 nC, f = 20 kHz, and T_{AMAX} = 85°C:

$P_E = 10\ mA \bullet 1.8V \bullet 0.8 = 14\ mW$

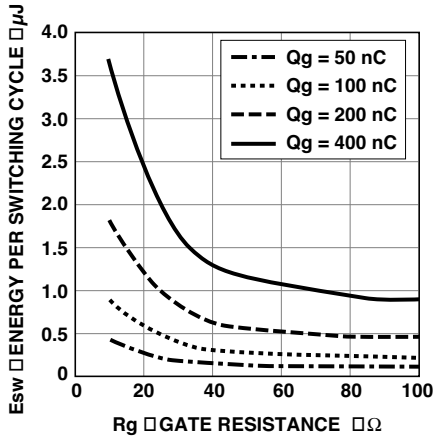
$P_O = (3\ mA + (0.001\ mA/(nC \bullet kHz)) \bullet 20\ kHz \bullet 100\ nC) \bullet 24V + 0.4\ \mu J \bullet 20\ kHz = 128\ mW$

$< 260\ mW\ (P_{O(MAX)}$ @ 85°C)

The value of 3 mA for I_{CC} in the previous equation is the max. I_{CC} over the entire operating temperature range.

Since P_O for this case is less than $P_{O(MAX)}$, Rg = 32Ω is alright for the power dissipation.

Figure 22: Energy Dissipated in the HCPL-314J and for Each IGBT Switching Cycle



LED Drive Circuit Considerations for Ultra-High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 23. The HCPL-314J improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5-8 as shown in Figure 24. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 21), can achieve 10-kV/μs CMR while minimizing component complexity.

Techniques to keep the LED in the proper state are discussed in the next two sections.

Figure 23: Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers

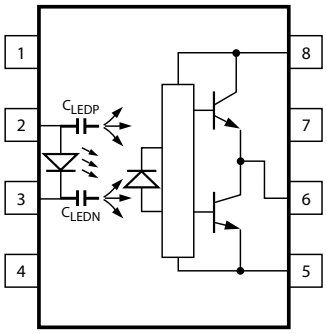


Figure 24: Optocoupler Input to Output Capacitance Model for Shielded Optocouplers

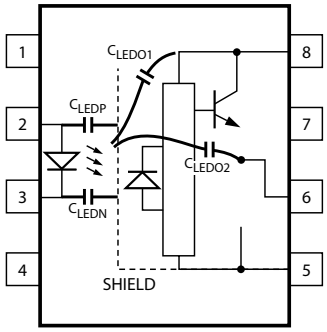


Figure 25: Equivalent Circuit for Figure 19 During Common Mode Transient

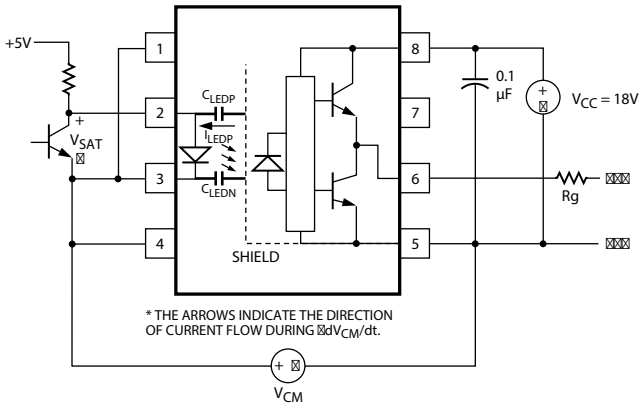


Figure 26: Not Recommended Open Collector Drive Circuit

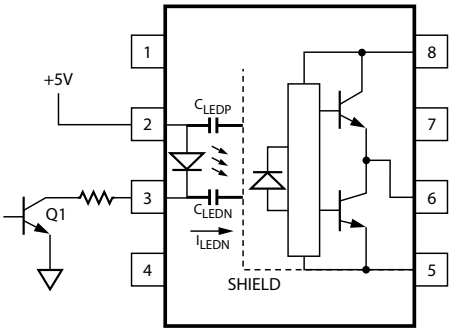
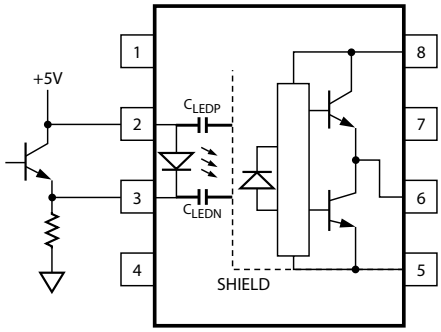


Figure 27: Recommended LED Drive Circuit for Ultra-High CMR IPM Dead Time and Propagation Delay Specifications



CMR with the LED On (CMR_H)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by over-driving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 8 mA provides adequate margin over the maximum I_{FLH} of 5 mA to achieve 10-kV/µs CMR.

CMR with the LED Off (CMR_L)

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $-dV_{CM}/dt$ transient in Figure 25, the current flowing through C_{LEDP} also flows through the R_{SAT} and V_{SAT} of the logic gate. As long as the low state voltage developed across the logic gate is less than $V_{F(OFF)}$, the LED will remain off and no common mode failure will occur.

The open collector drive circuit, shown in Figure 26, cannot keep the LED off during a $+dV_{CM}/dt$ transient, since all the current flowing through C_{LEDN} must be supplied by the LED, and it is not recommended for applications requiring ultra-high CMR_1 performance. The alternative drive circuit which like the recommended application circuit (Figure 21), does achieve ultra-high CMR performance by shunting the LED in the off state.

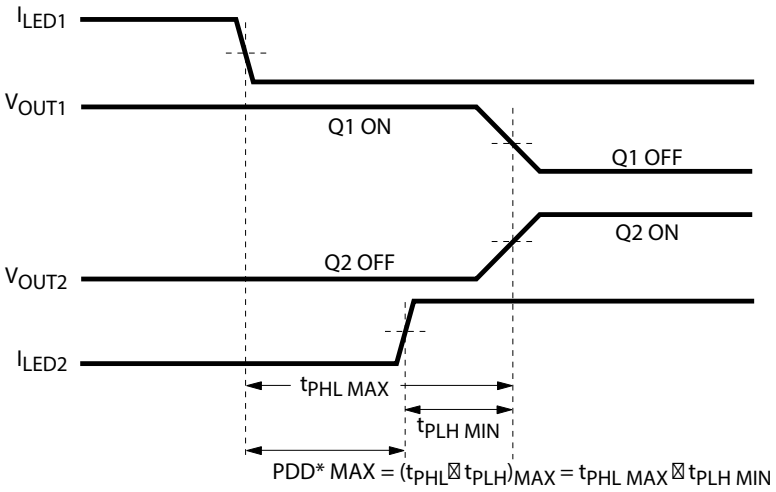
IPM Dead Time and Propagation Delay Specifications

The HCPL-314J includes a Propagation Delay Difference (PDD) specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time that high- and low-side power transistors are off. Any overlap in Ql and Q2 conduction will result in large currents flowing through the power devices from the high-voltage to the low-voltage motor rails. To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 28. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD max, which is specified to be 500 ns over the operating temperature range of –40° to 100°C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specification as shown in Figure 29. The maximum dead time for the HCPL-314J is 1 µs (= 0.5 µs – (–0.5 µs)) over the operating temperature range of –40°C to 100°C.

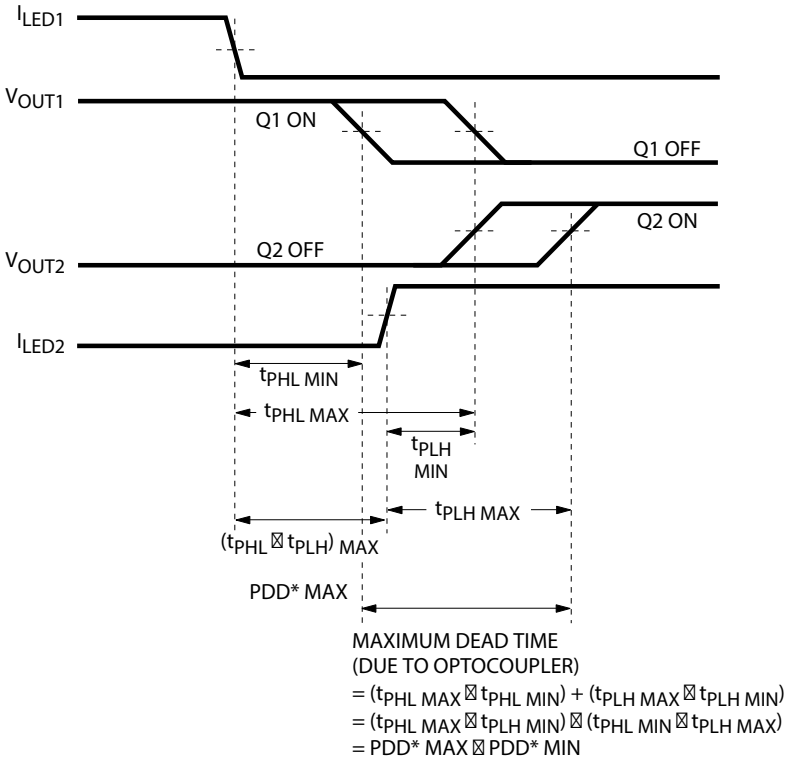
Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

Figure 28: Minimum LED Skew for Zero Dead Time



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR PDD CALCULATIONS, THE PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 29: Waveforms for Dead Time



*PDD = PROPAGATION DELAY DIFFERENCE
NOTE: FOR DEAD TIME AND PDD CALCULATIONS, ALL PROPAGATION DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

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